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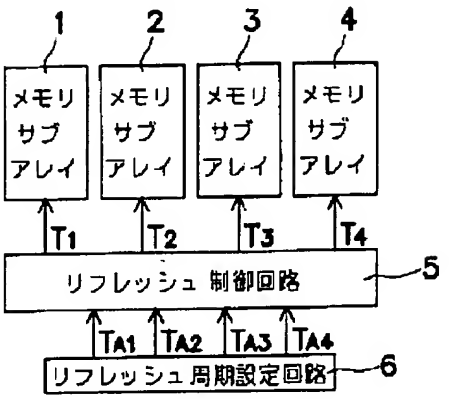
(54) DYNAMIC TYPE SEMICONDUCTOR MEMORY

(57) Abstract:

PURPOSE: To reduce power consumption by providing a individual refresh period setting means at every memory sub array.

CONSTITUTION: Respective memory sub arrays 1-4 are refreshed respectively by a refresh control circuit 5. The circuit 5 is a circuit generating the address for refreshing successively, selecting a word line and simultaneously refreshing by writing back again the stored data read from a memory cell connected to every word line. Further, the circuit 5 decides refresh periods T_1-T_4 so as to be satisfied with a relation I based on the refresh periods TA_1-TA_4 set by a refresh period setting circuit 6 and executes the refreshing operation of the arrays 1-4 with different periods based on these periods. Thus, the refresh period is set individually, since the array except the array having the longest refresh period unnecessitates an excess refresh operation, the power consumption is reduced.



$$\begin{cases} T_1 \leq T_{A1} \\ T_2 \leq T_{A2} \\ T_3 \leq T_{A3} \\ T_4 \leq T_{A4} \end{cases}$$